

REMARKS

This Amendment responds to the Office Action dated January 24, 2005 in which the Examiner rejected claims 1-12 under 35 U.S.C. §103.

As indicated above, claims 1 and 11 have been amended to make explicit what is implicit in the claims. The amendment is unrelated to a statutory requirement for patentability.

Claim 1 claims a leakage current reducing method of an LSI for reducing leakage current in an LSI chip divided into two parts; namely a main power supply region including circuits operated by receiving power from a main power source, and a backup power supply region including circuits operated by receiving power from a backup power source. The method comprises the steps of: connecting memory units in each of the circuits provided in the main power supply region through a scan path; starting a scanning operation, when the LSI chip is placed in an operation standby state, through the scan path, and reading information held in the memory units of each of the circuits provided in the main power supply region based upon a scan mode signal and a scanning clock pulse; and saving the information thus read by the scanning operation in a built-in storage section provided in the backup power supply region.

Through the method of the claimed invention reading information based upon a scan mode signal and a scanning clock pulse as claimed in claim 1, the claimed invention provides a leakage current reducing method of an LSI which can be carried out by a relative simple switching operation without the need for any special switching operation by a CPU. The prior art does not show, teach or suggest the invention as claimed in claim 1.

Claim 11 claims a leakage current reducing method of an LSI for reducing leakage current in an LSI chip divided into two parts; namely a main power supply region including circuits operated by receiving power from a main power source, and a backup power supply region including circuits operated by receiving power from a backup power source. The method comprises the steps of: disposing an external storage section operated by receiving power from the backup power source outside the LSI chip, and connecting memory units of each of the circuits provided in the main power supply region through a scan path; starting a scanning operation, when the LSI chip is placed in an operation standby state, through the scan path, serially reading information held in the memory units of each of the circuits provided in the main power supply region based upon a scan mode signal and a scanning clock pulse, converting the read serial information into parallel information, and then saving the parallel information in the external storage section by specifying addresses therefor; and parallelly reading, when the LSI chip is returned from the standby state, the information held in the external storage section by specifying addresses therefor, converting the read parallel information into serial information, and then setting the serial information in the memory units of each of the circuits provided in the main power supply region through the scan path.

Through the structure of the claimed invention reading information based upon a scan mode signal and a scanning clock pulse, as claimed in claim 11, the claimed invention provides a leakage current reducing method of a LSI without adding any SRAM units for storing scanned information inside the LSI chip. The prior art does not show, teach or suggest the invention as claimed in claim 11.

Claims 1-5, 7 and 9-10 were rejected under 35 U.S.C. § 103 as being unpatentable over Applicant's admitted prior art in view of *Tobias et al.* (U.S. Patent No. 6,363,501).

Applicant respectfully traverses the Examiner's rejection of the claims under 35 U.S.C. § 103. The claims have been reviewed in light of the Office Action, and for reasons which will be set forth below, Applicant respectfully requests the Examiner withdraws the rejection to the claims and allows the claims to issue.

Fig. 7 is a block diagram illustrating a reduction in leakage current in a system using the LSI of the related art. Here, an example of a system configuration using an LSI chip with a built-in CPU, and an external ROM, is specifically shown. In the drawing, a reference numeral 1 denotes an LSI chip; 2 an external ROM; 3 a main power source; 4 a main power supply and current cut-off switch; 5 a backup power source; and 6 a return trigger circuit. Inside the LSI chip 1, there are provided components including: a CPU 11; a CPU peripheral circuit 12; a data bus 13; an address bus/control signal line 14; a built-in SRAM 15; an internal current cut-off switch 16; and a power supply cut-off controller 17. A reference numeral 18 denotes a main power supply region; and 19 a backup power supply region. (page 1, line 26 through page 2, line 6) When the LSI chip 1 is placed in the standby state, causing power supplied to the CPU 11 and the CPU peripheral circuit 12 inside the main power supply region 18 to be cut off, information held in the memory units of the main power supply region thereof may be lost. Thus, before the power supplied from the main power source 3 is cut off, the information of each of such memory units is saved in the built-in SRAM 15 inside the backup power supply region 19. The saving of each of such stored information in the built-in SRAM 15 is carried out by the

switching operation of the CPU 11. After the power supplied from the power source 3 has been cut off, a portion to which power is being supplied is only the backup power supply region 19. (page 3, lines 18-30, emphasis added)

Thus, Applicant's admitted prior art merely discloses storing information from memory circuits into a built-in SRAM 15 through a data bus 13, address bus/control signal line 14 and internal current cut-off switch 16. Nothing in Applicant's admitted prior art shows, teaches or suggests reading information based upon a scan mode signal and a scanning clock pulse as claimed in claim 1. Rather, Applicant's admitted prior art merely discloses storing the information via a data bus 13, address bus 14 and cutoff switch 16.

Tobias et al. appears to disclose peripheral states registers embedded in a microcontrollers, and more specifically, using scan hardware to capture peripheral device states. (col. 1, lines 10-12) FIG. 2 illustrates typical peripheral devices embedded in a microcontroller M with a scan path. An input pin IN of microcontroller M is provided to shift configuration data into each peripheral configuration register. The configuration registers of the clock and power management unit 102, interrupt control unit 106, timer control unit 110, DMA unit 114, PIO unit 132, asynchronous serial port 136, synchronous serial port 140, chip select unit 126 and bus interface unit 118 are daisy chained together via signal line SCAN_PATH. For illustrative purposes, the SCAN_PATH line from the output of the bus interface unit configuration registers 120a is coupled to the output pin OUT of the microcontroller M. Data is synchronously shifted in or out of each configuration register utilizing clock CLK_SCAN. The data out pin OUT is coupled to an external memory 200. Thus, the configuration data from each peripheral device is sequentially shifted out of

each configuration register into external memory 200 via SCAN_PATH. Likewise, the external memory 200 is coupled to the input pin IN, so that data from external memory 200 can be synchronously shifted into each peripheral configuration register via SCAN_PATH. (col. 4, lines 19-40)

Thus, *Tobias et al.* merely discloses data is synchronously shifted in or out utilizing clock CLK_SCAN. However, as claimed in claim 1, the information is read based upon a scan mode signal and a scanning clock pulse. However, *Tobias et al.* teaches away from the claimed invention since the data from the peripheral device is sequentially shifted out into an external memory 200 via the scan path based on clock CLK_SCAN..

Since neither Applicant's admitted prior art or *Tobias et al.* show, teach or suggest reading information based upon a scan mode signal and a scanning clock pulse as claimed in claim 1, Applicant respectfully requests the Examiner withdraws the rejection to claim 1 under 35 U.S.C. §103.

Claims 2-5, 7 and 9-10 depend from claim 1 and recite additional features. Applicant respectfully submits claims 2-5, 7 and 9-10 would not have been obvious within the meaning of 35 U.S.C. § 103 over Applicant's admitted prior art and *Tobias et al.* at least for the reasons as set forth above. Therefore, Applicant respectfully requests the Examiner withdraws the rejection to claims 2-5, 7 and 9-10 under 35 U.S.C. § 103.

Claims 6 and 11-12 were rejected under 35 U.S.C. § 103 as being unpatentable over Applicant's admitted prior art and *Tobias et al.* and further in view of *Goldstein* (U.S. Patent No. 6,684,275).

Applicant respectfully traverses the Examiner's rejection of the claims under 35 U.S.C. § 103. The claims have been reviewed in light of the Office Action, and for reasons which will be set forth below, Applicant respectfully requests the Examiner withdraws the rejection to the claims and allows the claims to issue.

As discussed above, nothing in Applicant's admitted prior art or *Tobias et al.* shows, teaches or suggests reading information based upon a scan mode signal and a scanning clock pulse as claimed in claim 11.

Goldstein appears to disclose a method for converting serial bit streams into parallel bit streams and visa versa. (col. 1, lines 14-16) In systems using multiple serial streams it becomes necessary to create a digital switch that is capable of transmitting data from a time-slot on one stream onto either a different timeslot on the same stream or onto another stream altogether. As the number of serial TDM streams increases, these switching devices usually convert the serial TDM streams into a parallel TDM stream internally to the device. This makes it easier to store the data in memory. If the data on the streams is to be processed by a computer, again the data must be converted from serial to parallel form. Often a single stream serial-to-parallel converter is incorporated into the computer. The serial port is connected to a switching device and other streams are then connected to the TDM highway. These two concepts can be combined so that data taken from the TDM highway is converted to parallel and stored in a memory device (e.g., a RAM) for use by the processor. The processor also places data to be transmitted on the TDM highway into the memory device, and the circuit converts this data from parallel to serial. (col. 1, line 51 through col. 2, line 3)

Thus, *Goldstein* merely discloses converting data from serial information into parallel information and vice versa. Nothing in *Goldstein* shows, teaches or suggests reading information based upon a scan mode signal and a scanning clock pulse as claimed in claim 11. Rather, *Goldstein* merely discloses converting data from serial to parallel or vice versa.

Since nothing in Applicant's admitted prior art, *Tobias et al.* or *Goldstein* show, teach or suggest reading information based upon a scan mode signal and a scanning clock signal pulse as claimed in claim 11, Applicant respectfully requests the Examiner withdraws the rejection to claim 11 under 35 U.S.C. §103.

Claim 6 depends from claim 1 and claim 12 depends from claim 11 and recite additional features. Applicant respectfully submits that claims 6 and 12 would not have been obvious within the meaning of 35 U.S.C. § 103 over Applicant's admitted prior art, *Tobias et al.* and *Goldstein* at least for the reasons as set forth above. Therefore, Applicant respectfully requests the Examiner withdraws the rejection to claims 6 and 12 under 35 U.S.C. § 103.

Claim 8 was rejected under 35 U.S.C. § 103 as being unpatentable over Applicant's admitted prior art, *Tobias et al.* and *Masabumi et al.* (Japanese Reference 5-108194).

Applicant respectfully traverses the Examiner's rejection of the claim under 35 U.S.C. § 103. The claim has been reviewed in light of the Office Action, and for reasons which will be set forth below, Applicant respectfully requests the Examiner withdraws the rejection to the claim and allows the claim to issue.

As discussed above, since nothing in Applicant's admitted prior art and *Tobias et al.* show, teach or suggest the primary features as claimed in claim 1, Applicant

respectfully submits that the combination of the primary references with the secondary reference to *Masabumi et al.* would not overcome the deficiencies of the primary references. Therefore, Applicant respectfully requests the Examiner withdraws the rejection to claim 8 under 35 U.S.C. § 103.

Thus it now appears that the application is in condition for reconsideration and allowance. Reconsideration and allowance at an early date are respectfully requested. Should the Examiner find that the application is not now in condition for allowance, Applicant respectfully requests the Examiner enters this amendment for purposes of appeal.

If for any reason the Examiner feels that the application is not now in condition for allowance, the Examiner is requested to contact, by telephone, the Applicant's undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed within the currently set shortened statutory period, Applicant respectfully petitions for an appropriate extension of time. The fees for such extension of time may be charged to our Deposit Account No. 02-4800.

In the event that any additional fees are due with this paper, please charge
our Deposit Account No. 02-4800.

Respectfully submitted,

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